

**CLAIM AMENDMENTS:**

1. (Currently Amended) A method for etching a capacitor structure within a silicon substrate, said method comprising:

providing a masked substrate comprising a patterned masking layer over said silicon substrate, said patterned masking layer having at least one aperture formed therein;

performing a series of ~~at least two~~ process steps upon said ~~masked substrate~~ silicon substrate through said at least one aperture in said patterned masking layer, said series of ~~at least two~~ process steps comprising (a) an isotropic plasma etching step in which said silicon substrate is etched ~~through said at least one aperture~~; and (b) a plasma deposition step in ~~which a passivating layer is deposited on said silicon substrate~~; and

repeating said series of ~~at least two~~ process steps until a desired etch depth for said capacitor structure is achieved, wherein said capacitor structure has ~~comprises an~~ etched sidewall with ~~an undulating profile that has an increased surface area relative to a smooth sidewall~~.

2. (Original) The method according to claim 1 wherein said capacitor structure ranges from 1-10.0 microns in vertical dimension.

3. (Currently Amended) The method according to claim 1, wherein said capacitor structure is a trench structure.

4. (Original) The method according to claim 1 wherein said capacitor structure is an elevated structure.

5. (Cancelled) ~~The method according to claim 1 wherein said series of at least two process steps comprises (1) an isotropic plasma etching step and (2) an anisotropic plasma etching step.~~

6. (Cancelled) ~~The method according to claim 1 wherein said series of at least two steps comprises (1) an isotropic plasma etching step and (2) a plasma deposition step in which a passivating layer is deposited on said substrate.~~

7. (Cancelled) ~~The method according to claim 5 wherein said isotropic etching step is performed in the presence of a source gas comprising one or more of SF<sub>6</sub>, Cl<sub>2</sub>, NF<sub>3</sub> and CF<sub>4</sub>,~~

8. (Cancelled) ~~The method according to claim 7 wherein said isotropic etching step is performed in the presence of a source gas comprising SF<sub>6</sub>.~~

9. (Cancelled) ~~The method according to claim 5 wherein said anisotropic etching step is performed in the presence of a plasma source gas comprising SF<sub>6</sub>, HBr and O<sub>2</sub>.~~

10. (Cancelled) ~~The method according to claim 9 wherein a SF<sub>6</sub>:HBr:O<sub>2</sub> ratio is about 1:1:1.~~

11. (Currently Amended) The method according to ~~claim 6~~ claim 1 wherein said isotropic etching step is performed in the presence of a source gas comprising one or more of SF<sub>6</sub>, Cl<sub>2</sub>, NF<sub>3</sub> and CF<sub>4</sub>.

12. (Currently Amended) The method according to ~~claim 6~~ claim 1 wherein said isotropic etching step is performed in the presence of a source gas comprising SF<sub>6</sub>.

13. (Currently Amended) The method according to ~~claim 6~~ claim 1 wherein said deposition step is performed in the presence of a source gas comprising a fluorocarbon gas or a fluorohydrocarbon gas.

14. (Currently Amended) The method according to ~~claim 6~~ claim 1 wherein said deposition step is performed in the presence a source gas comprising of one or more of C<sub>4</sub>F<sub>8</sub>, CH<sub>2</sub>F<sub>2</sub>, CHF<sub>3</sub>, and C<sub>4</sub>F<sub>6</sub>.

15. (Currently Amended) The method according to ~~claim 6, claim 1~~ wherein said deposition step is performed in the presence of a source gas comprising C<sub>4</sub>F<sub>8</sub>.

16. (Original) The method according to claim 1 wherein said etching step is conducted at a plasma density ranging from 10<sup>11</sup> to 10<sup>12</sup> cm<sup>-3</sup>.

17. (Original) The method according to claim 1 wherein said etching step proceeds at a rate ranging from 1-3 microns per minute.

18. (Withdrawn) A capacitor structure formed by a process comprising:  
providing a masked substrate comprising a patterned masking layer over said silicon substrate, said patterned masking layer having at least one aperture formed therein;  
performing a series of at least two process steps upon said masked substrate, said series of at least two process steps comprising an isotropic plasma etching step in which said silicon substrate is etched through said at least one aperture; and  
repeating said series of at least two process steps until a desired etch depth for said capacitor structure is achieved, wherein said capacitor structure has etched sidewall with a undulating profile.

19. (Withdrawn) The capacitor structure according to claim 18, wherein said capacitor structure ranges from 1-10.0 microns in vertical dimension.

20. (Withdrawn) The capacitor structure according to claim 18, wherein said capacitor structure is a trench.

21. (Withdrawn) The capacitor structure according to claim 18, wherein said capacitor structure is one of a portion of a stacked capacitor and a trench capacitor.

22. (Withdrawn) The capacitor structure according to claim 18, wherein said series of at least two process steps comprises (1) an anisotropic plasma-etching step and (2) an isotropic plasma-etching step.

23. (Withdrawn) The capacitor structure according to claim 18 wherein said series of at least two process steps comprises (1) an isotropic plasma etching step and (2) a plasma deposition step in which a passivating layer is deposited on said substrate.

24. (Newly added) The method according to claim 1, wherein said capacitor structure is a trench structure, wherein said isotropic etching step is performed in the presence of a source gas comprising SF<sub>6</sub>, and wherein said deposition step is performed in the presence of a source gas comprising C<sub>4</sub>F<sub>8</sub>.